ENSURING ELECTROMAGNETIC COMPLIANCE IN PRINTED CIRCUIT BOARDS THROUGH DESIGN FOR ASSEMBLY GUIDELINES

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ABSTRACT

The aim of this work is to provide the embodiment of sample PCB design for manufacturing and assembly rules for fine-pitch devices in a commercially PCB design application. Most commercially used PCB design applications provide for PCB design rule-checking to an extent, particularly in setting geometric constraints for laying out components on the substrate. For example, in automatic placement of connectors and components within a PCB design file. The role of the design rule checker within PCB design software is a fundamentally important in ensuring process yield in PCB fabrication as well as ensuring functional acceptance in test whilst maintaining accurate placement of components.

The design rules implemented in this paper emanate from a wider programme of research that focusses on design for manufacturing and assembly issues in Surface Mount Technology (SMT), Fine-Pitch Technology (FPT) and Flat Pack Ball-Grid Array (FPBGA). This work explores the methodology of decision support in the design of electronic products with specific regard to design for manufacturing and assembly. The design for manufacturing rules used in this implementation scenario is for the precise location and placement of Fine-pitch components.

1 DESIGN REQUIREMENTS FOR ULTRA FINE-PITCH DEVICES

In order to control overall area requirements for the higher pin-count devices, component manufacturers have reduced the lead pitch (the space between lead centres). The standard family of the Standard Quad Flat-Pack (SQFP) has been adopted by the industry to provide commercial packaging of custom and semi-custom integrated circuits with 0.65mm, 0.5mm, 0.4mm and 0.3mm lead pitch. Although assembly processing has been refined to acceptable yields levels for 0.65mm and 0.5mm pitch device types, conventional process methods might not be practical for high pin count using the 0.4mm and 0.3mm pitch devices [1]. While adapting this advanced packaging technology, the users of the SQFP are challenged by several considerations, including physical, financial and environmental issues. Physical issues include attachment processes and finished product reliability. Figure 1 illustrates the design guidelines and rules that require to be considered and adhered to in the design for fabrication and assembly of fine-pitch PCBs.

Specific reference is made to abbreviations such as CSG1…CSG10 these correspond to discrete fine-pitch design rules which have been coded into a knowledge-based decision-support tool. This was the main deliverable from the research programme from which Figure 1 was taken.

1.1 Designing the Substrate for Fine-Pitch Assembly

Many factors have impact upon assembly yield as well as solder joint quality. Each of the following elements must be carefully reviewed and calculated so as to ensure ease of assembly. Formulation the land pattern array and calculate geometry such that devices are placed exactly on the solder lands. Implementation of the test model substrate design layout so as to ensure that the fabrication detail is to specification prior to assembly. The small SQFP devices are manufactured in high volume and provide rugged, long-term reliability. Newer packages in the industry, such as the 0.4mm (0.016-in) lead pitch SQFP might pose a challenge to manufacturers in maintaining a consistent assembly process yield [1].

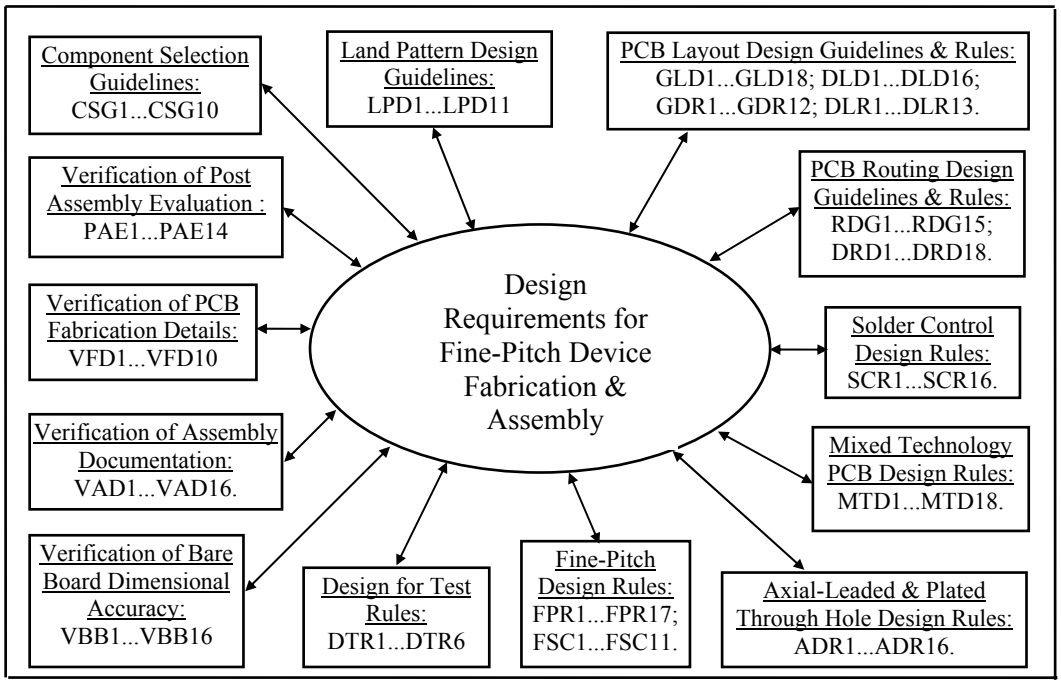

Figure 1: A Model of Knowledge-Based Decision Support in PCB Design for Assembly

1.2 Typical Fine-Pitch Device Package Description

The EIAJ standard SQFP 256-pin configuration on 0.4mm (0.016-in) pitch provides adequate termination channels for more advanced ASIC devices while requiring a relatively small area for attachment. The total surface area (lead end to end) of the 256-lead plastic device is less than 31.0mm (1.22-in) square with a maximum height from the substrate surface of 3.5mm (0.137-in). The leads are formed in the gull-wing configuration extending from the device body providing a contact area of 0.5mm±.0.2mm (0.02-in±0.008-in) [1]. For a process development or test program, a non-functional component can be ordered with internal bonding on lead pairs before moulding.

1.3 Design Allowance for Physical Tolerances of Devices

Although the lead-pitch tolerance can be defined as non-accumulative, the width of the lead at the attachment area is specified as wide as ±0.07mm (0.003-in). Using the maximum material condition of the basic lead width of 0.15mm opens the possibility for up to 0.22mm total lead width. The final land pattern geometry provided on the substrate must accommodate this maximum material condition of the device so as to avoid the possibility of lead overlap at either the toe or heel of the J-lead termination. The land pattern geometry and spacing between pad rows are derived from calculating both the maximum and minimum material conditions of the device. That is, if the device is supplied at the maximum overall width (lead end to lead end), the land pattern should provide enough surface area to prevent lead overhang [1].

1.4 The Impact that Design Has on Assembly Efficiency of Fine-Pitch SMT PCBs

Seventy percent of the failures detected on surface mount assemblies are due to solder defects. Solder defects found at test are either in the form of a short between device leads or open circuits due to insufficient solder [2]. An ongoing process audit can reduce most of the solder defects but often manufacturing problems are design related and if not corrected will remain a source of chronic failure. By the implementation of proven circuit board design rules it is possible further reduce solder defects. These rules specifically employ process-compatible land pattern geometries for surface mount devices and each will play a significant role in ensuring manufacturing efficiency and quality. The design rules will also focus on PCB fabrication guidelines and assembly machine compatibility. Land pattern geometry on the other hand is directly related to process control and solder attachment uniformity. When each of these primary disciplines are properly defined and implemented all solder defects can be eliminated. Solder defects can be further reduced through continued process refinement. Each process step must be monitored by means of human or automated visual inspection during the initial start-up of a product, 100% inspection is not uncommon. After process stabilisation, only sampling of the assembly is needed. As each unit is inspected, defects exceeding standard limits are identified and recorded. The defect ratio from one assembly to the other does not seem to be affected by the reflow process as much as the solder paste characteristics [3]. The viscosity of the solder paste will have a more significant impact on the solder joint defect ratio of the 0.4-0.5mm (0.016-0.020-in) devices.

Although the solder volume of each joint can be mathematically modelled, visual inspection on the finer pitch devices is not without compromise. A 100%

inspection of every lead on the finer pitch devices is not practical and the use of advanced inspection systems for fine-pitch devices is inevitable. For example, ultrasonic imaging, X-ray and X-ray laminography might prove to be very effective in performing a non-destructive solder quality certification to measure solder density of detection of solder voids [4]. Solder paste registration for the majority of the surface mount devices can be improved, for example, by reducing the overall stencil opening and to compensate for all the tolerance variables of a typical PCB, a reduction of the stencil opening by 10-20% might be adequate.

1.5 Placement Accuracy and Land Pattern Design Requirements

Less-than-perfect machine placement of passive and 1.27mm (0.050-in) pitch surface mount devices can be tolerated to a limited extent. As during the reflow-soldering process the entire assembly is heated to approximately 200°c and the solder paste is converted to a liquid state. These devices are momentarily suspended in the liquid alloy and through surface tension, the device mass will tend to self-centre before the solder begins to cool. This phenomenon while predictable for passive and coarse-pitch devices, cannot be relied upon for fine-pitch attachment as the land pattern geometry is much more critical. The land pattern geometry must provide for both the minimum and maximum material condition of the device and substrate [5]. The designer must calculate the basic land pattern limits with provision for inspection and machine placement tolerances.

2 USING PCB DESIGN RULES WITHIN PCB DESIGN SOFTWARE

With PCB design software the PCB is designed by the placement of components, tracks, vias and other design objects. These objects must be placed in the workspace with close regard to each other. Components must not overlap, nets must not short, power nets must be kept clear of signal nets, etc. To allow the designer to remain focused on the task of designing the board, a design rule checker can monitor such design requirements. These design rules are monitored as the designer lays out the PCB. As soon as an object is placed in violation of a design rule it is highlighted.

3 AN IMPLEMENTATION OF PCB ROUTING DESIGN GUIDELINES FOR EMC

A PCB was selected for the implementation of such design rules it was a digital-to-analogue converter board used in a radio frequency product. The design of the PCB was constrained by the product envelope and therefore had to very small in size, specifically 40mm by 75mm. The fine-pitch devices used in this design had lead-pitch of 0.4mm. Owing to the fact that the product was a radio frequency application, specific attention was made to design for Electro-Magnetic Compatibility (EMC). EMC is characterised by capacitive and inductive reactions within signal traces because such traces can act as unintentional wave-guides for the reception and transmission of radio frequency signals. These reactions are often referred to as electrical noise and PCB designers are required to exercise caution in laying out components and routing traces on PCBs so as to minimise such noise.

To ensure that the PCB was EMC compliant specific design rules pertaining to signal trace-widths and corresponding air-gaps between traces need to be adhered to. As a rule of thumb for EMC, the design-rule checker needs to be instructed that signal traces cannot be less than 0.13mm wide and the gap between signal traces must not exceed 0.13mm. Moreover, for power and ground planes namely VCC and GND the respective trace-width cannot be less that 0.2mm and the gap between such traces must not exceed 0.2mm. With reference to PCB Routing Design Guidelines it is possible to implement such rules within the routing design rule class, under width constraint and clearance constraint (see Table 1). Table 1 shows the definitions of the design rules for width constraint and clearance constraint, it explains what happens when a design-rules violation occurs and explains when the design rule can be invoked by the designer.

The implementation of PCB routing rules Figures 1 and 2 respectively. Figures 1 and 2 are design-rule entry dialogs for 'Routing Width Constraint' and 'Clearance Constraint' design rules respectively.

Routing Width Constraint design rule	**Clearance Constraint design rule**
Rule class: Routing	**Rule class: Routing**
Defines the minimum and maximum width of tracks and arcs on the copper layers. **How Duplicate Rule Contentions are Resolved**: The rule with the tightest range is obeyed.	Defines the minimum clearance allowed between any two primitive objects on a copper layer. Use the Clearance Constraint to ensure that routing clearances are maintained. The Connective Checking option would typically be set to Different Nets. An example of when Any Net could be used is to test for vias being placed too close to pads or other vias on the same net, or any other net. **How Duplicate Rule Contentions are Resolved**: The rule with the largest clearance is obeyed.
Rule Application: During auto-routing and Batch DRC.	**Rule Application**: On-line DRC, Batch DRC and during auto-routing.

Table 1: Routing Width Constraint and Routing Clearance Constraint Design Rules.

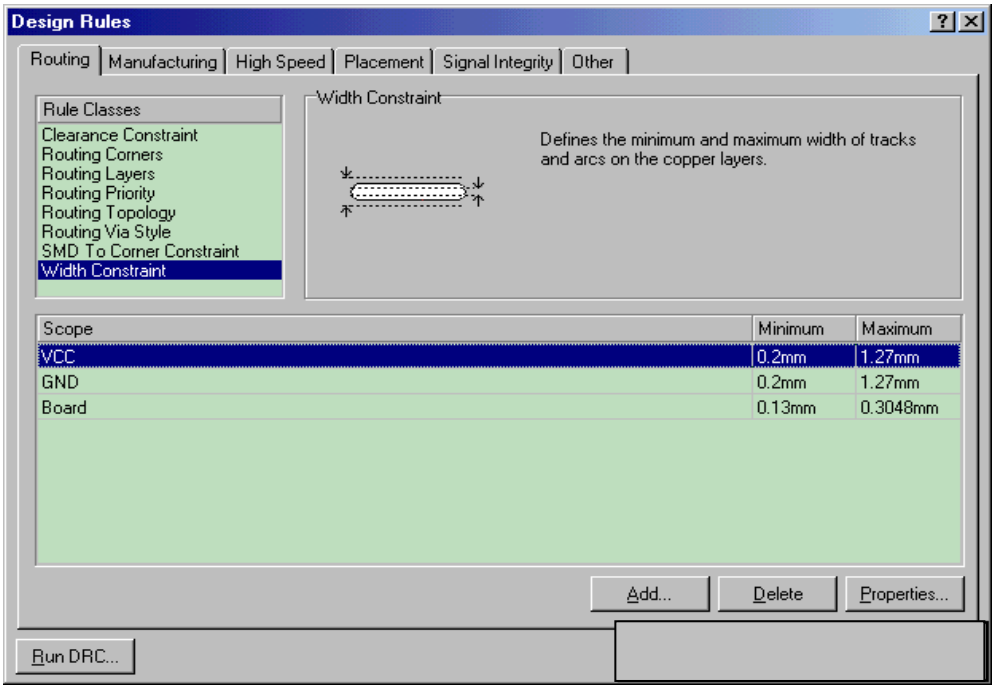

Figure 1: Rule Implementation in PCB Routing Width Constraint Rule-Check Dialog

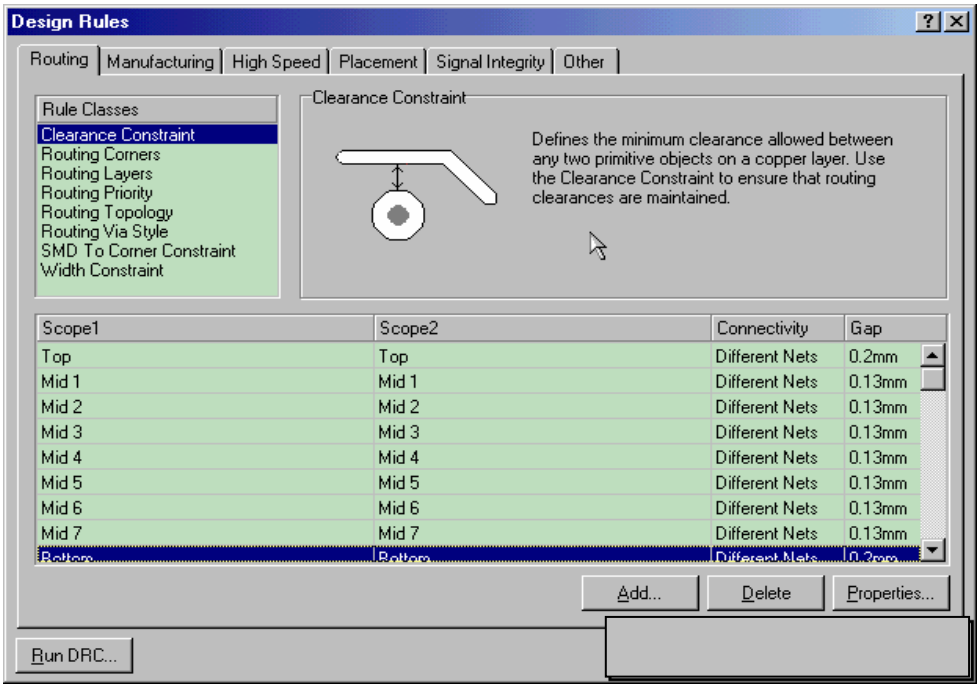

Figure 2: Rule Implementation in PCB Clearance Constraint Rule-Check Dialog

4 CONCLUSION

This paper demonstrated the implementation of sample fine-pitch PCB design rules in an existing PCB design file. The design rules implemented were a sample of those guidelines and rules represented selected from a programme of wider study in design for assembly in PCB design. This sample was selected on the basis that these design rules lent themselves to quantitative and geometric representation. Those PCB design rules that were implemented included: routing design guidelines; layout design rules; and device oriented layout rules. The PCB design-rule editor is instructed of such design requirements by the setting up of a series of design rules. Also, during the board verification process, an integrated design rule checker can be executed which will generate a report of any design rule violations on the PCB.

5 REFERENCES

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